ABSTRACT OF THE DISCLOSURE

A gate electrode layer is doped in a first section of a semiconductor substrate. By means of a patterning, encapsulated gate electrodes emerge from the gate electrode layer, which gate electrodes are arranged in a high packing density in a first section and are assigned to selection transistors of memory cells, and are arranged in a low packing density in a second section and are assigned to transistors of logic circuits. After a processing of the selection transistors, the encapsulated gate electrodes are uncovered in the second section and are subsequently doped in the same way in each case simultaneously with the respectively assigned source/drain regions. Together with a subsequent siliciding of the gate electrodes and of the source/drain regions, the performance of the transistors in the second section is significantly increased with little additional outlay.